

(19) World Intellectual Property  
Organization  
International Bureau



(43) International Publication Date  
16 June 2005 (16.06.2005)

PCT

(10) International Publication Number  
**WO 2005/055611 A1**

(51) International Patent Classification<sup>7</sup>: **H04N 7/26**

(21) International Application Number:  
PCT/GB2004/004924

(22) International Filing Date:  
23 November 2004 (23.11.2004)

(25) Filing Language: English

(26) Publication Language: English

(30) Priority Data:  
03257455.0 26 November 2003 (26.11.2003) EP

(71) Applicants (for all designated States except US): **STMI-CROELECTRONICS LIMITED** [GB/GB]; 1000 Aztec West, Almondsbury, Bristol BS32 4SQ (GB). **STMICRO-ELECTRONICS Srl** [IT/IT]; Via Olivetti 2, I-20041 Agrate Brianza (IT).

(72) Inventors; and

(75) Inventors/Applicants (for US only): **BOLTON, Martin** [GB/GB]; Lake House, Grib Lane, Blagdon BS40 7SA (GB). **CARRANO, Michele** [IT/IT]; via Giuseppe Verdi, N.53, I-95129 Catania (IT).

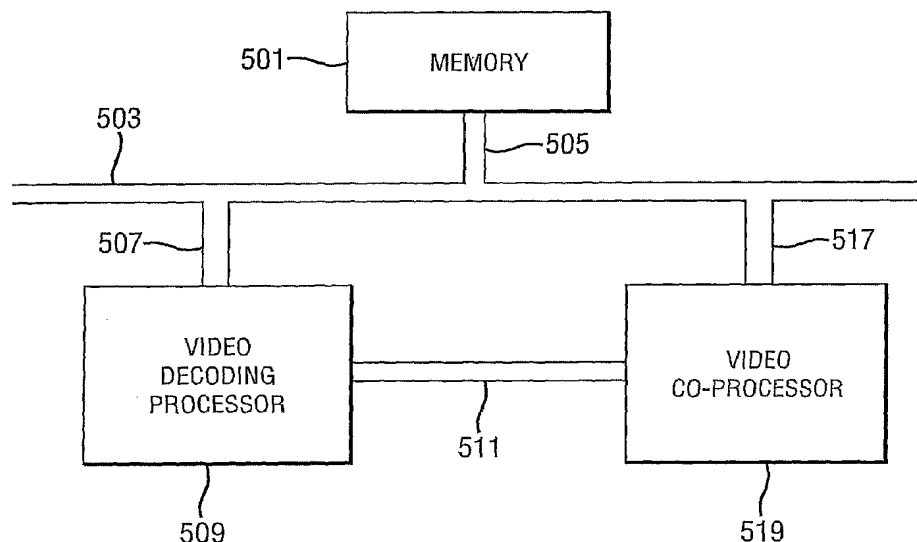
(74) Agents: **STYLE, Kelda, Camilla, Karen** et al.; Page White & Farrer, 54 Doughty Street, London WC1N 2LS (GB).

(81) Designated States (unless otherwise indicated, for every kind of national protection available): AE, AG, AL, AM, AT, AU, AZ, BA, BB, BG, BR, BW, BY, BZ, CA, CH, CN, CO, CR, CU, CZ, DE, DK, DM, DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, HR, HU, ID, IL, IN, IS, JP, KE, KG, KP, KR, KZ, LC, LK, LR, LS, LT, LU, LV, MA, MD, MG, MK, MN, MW, MX, MZ, NA, NI, NO, NZ, OM, PG, PH, PL, PT, RO, RU, SC, SD, SE, SG, SK, SL, SY, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, YU, ZA, ZM, ZW.

(84) Designated States (unless otherwise indicated, for every kind of regional protection available): ARIPO (BW, GH, GM, KE, LS, MW, MZ, NA, SD, SL, SZ, TZ, UG, ZM, ZW), Eurasian (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European (AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HU, IE, IS, IT, LU, MC, NL, PL, PT, RO, SE, SI, SK, TR), OAPI (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, ML, MR, NE, SN, TD, TG).

[Continued on next page]

(54) Title: A VIDEO DECODING DEVICE



(57) Abstract: A video decoding circuit comprising: a first video data processor; a second video data processor; and a connection connecting the first video data processor and the second data processor; wherein the first video data processor is arranged to receive a first signal comprising encoded video data, process the first signal to provide a second signal and output said second signal. The first video data processor being arranged to process the first signal dependent on at least part of the received first signal. The second video data processor is arranged to receive at least a part of the second signal, process the at least a part of the second signal to provide a third signal, and output the third signal, the second and third signals comprising a decoded video image stream. The second video data processor is arranged to process the at least part of the second signal dependent on at least part of the at least part of second signal.

WO 2005/055611 A1



---

**Published:**

- with international search report
- with amended claims

*For two-letter codes and other abbreviations, refer to the "Guidance Notes on Codes and Abbreviations" appearing at the beginning of each regular issue of the PCT Gazette.*